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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,981	10/20/2003	Beom-jun Jin	5649-1135	8976

20792 7590 10/01/2008
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
KARIMY, MOHAMMAD TIMOR	
ART UNIT	PAPER NUMBER
2894	

MAIL DATE	DELIVERY MODE
10/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,981	JIN, BEOM-JUN	
	Examiner	Art Unit	
	MOHAMMAD Timor KARIMY	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "**the** conductive contact" in line 16. There is insufficient antecedent basis for this limitation in the claim.

Claim 31 recites the limitation "**the** conductive contact" in line 16. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims10 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koga et al. (US Patent 6,649,500 B2) and Igarashi et al. (US Patent 6,838,732 B2), and in further view of Yokoyama (US Patent 6,703,715 B2).

With respect to claim 10, Koga teaches in figures 1-11(d) an integrated circuit device comprising:

an integrated circuit substrate (column 14, lines 32-33) in which source/drain regions 208 are formed;

a first interlevel dielectric layer 210 which is formed on the integrated circuit substrate;

gate line patterns 203 which are formed in the first interlevel dielectric layer;

first contact spacers 207 which are formed along the side walls of the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers 209 which formed of silicon nitride and formed on the first contact spacers; and

contact plugs 213a which are present in the contact holes between the second contact spacers.

However, Koga does not explicitly teach contact pads between adjacent gate line patterns and connected to the source/drain regions. Nonetheless, Igarashi teaches in figure 16, wherein a silicide contact pad 105 is positioned to make an ohmic contact with a diffusion layer 104 underneath. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Koga by using a silicide contact pad as taught by Igarashi in the interest of an ohmic contact with the diffusion layer 208 underneath (note that the silicide contact pad (5,105) in Ingrashi's device has a larger width than a conductive plug (6, 106 - Fig. 7 & 16); as such, one employed in Koga's

device, the silicide contact pad as taught by Ingrashi will have a larger width than Koga's conductive plug and will be in contact with the first contact spacer (207, 102) , which will prevent the second contact spacer (209, 109 – Koga's Fig. 10(d) & 6(c)) contacting the silicide contact pad). The motivation for using ohmic contact is known in the art to be low-resistance and stable contacts that improve the performance and reliability of integrated circuit devices. Therefore, Koga and Igarashi are combinable.

Moreover, Koga does not explicitly teach a second interlevel dielectric layer on the first interlevel dielectric layer having a via hole. Nonetheless, the use of stacked interlevel dielectric layers is commonly known in the semiconductor metallization structures. For instance, Yokoyama teaches in figure 5 interlevel dielectric layers 30 & 34a-b to provide insulation between neighboring elements. Moreover, the interlevel dielectric layers have via holes for electrical connection between the various levels. As such, the use of a second and/or third interlevel dielectric layers having contact holes is known to a person of ordinary skill in the art.

With respect to claim 31, Koga teaches in figures 1-11(d) an integrated circuit device comprising:

an integrated circuit substrate (column 14, lines 32-33) in which source/drain regions 208 are formed;

a first interlevel dielectric layer 210 which is formed on the integrated circuit substrate;

gate line patterns 203 which are formed in the first interlevel dielectric layer;

first contact spacers 207 which are formed along the side walls of the contact holes, the first contact spacers being formed of silicon oxide;

second contact spacers 209 which formed of silicon nitride and formed on the first contact spacers; and

contact plugs 213a which are present in the contact holes between the second contact spacers.

However, Koga does not explicitly teach contact pads between adjacent gate line patterns and connected to the source/drain regions. Nonetheless, Igarashi teaches in figure 16, wherein a silicide contact pad 105 is positioned to make an ohmic contact with a diffusion layer 104 underneath. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Koga by using a silicide contact pad as taught by Igarashi in the interest of an ohmic contact with the diffusion layer 208 underneath (note that the silicide contact pad (5,105) in Ingrashi's device has a larger width than a conductive plug (6, 106 - Fig. 7 & 16); as such, one employed in Koga's device, the silicide contact pad as taught by Ingrashi will have a larger width than Koga's conductive plug and will be in contact with the first contact spacer (207, 102) , which will prevent the second contact spacer (209, 109 – Koga's Fig. 10(d) & 6(c)) contacting the silicide contact pad). The motivation for using ohmic contact is known in the art to be low-resistance and stable contacts that improve the performance and reliability of integrated circuit devices. Therefore, Koga and Igarashi are combinable.

Moreover, Koga does not explicitly teach a second interlevel dielectric layer on the first interlevel dielectric layer having a via hole. Nonetheless, the use of stacked interlevel dielectric layers is commonly known in the semiconductor metallization structures. For instance, Yokoyama teaches in figure 5 interlevel dielectric layers 30 & 34a-b to provide insulation between neighboring elements. Moreover, the interlevel dielectric layers have via holes for electrical connection between the various levels. As such, the use of a second and/or third interlevel dielectric layers having contact holes is known to a person of ordinary skill in the art.

Response to Arguments

5. Applicant's arguments filed 06/24/2008 with respect to claims 10 and 31 have been considered but they are not persuasive.

Examiner submits that while Ingrashi discusses a conventional art in Fig. 16; nonetheless, Ingrashi continues discussing a silicide layer between a conductive plug and diffusion regions to introduce ohmic contacts. Examiner respectfully disagrees with applicant and maintains that the advantages of ohmic contacts are well-known in the art. It is within one of ordinary skill in the art's understanding to use ohmic contact at metal/semiconductor junctions in order to obtain an electrical contact having low resistance and improved stability. This ohmic contact characteristic has direct effects on the operation and reliability of a semiconductor device.

Examiner submits that Koga's gate line pattern (Fig. 10d) is formed in first interlayer dielectric layer 210, and examiner agrees with applicant that a silicide contact

pad is not positioned in a first dielectric layer; however, applicant's claim language does not reflect applicant's argument. Based on the broad presentation of this feature in the claim, examiner has interpreted the gate line patterns being in the first dielectric layer.

Additionally, examiner would like to point out that the silicide contact pad (5,105) in Ingrashi's device has a larger width than a conductive plug (6, 106 - Fig. 7 & 16); as such, one employed in Koga's device, the silicide contact pad as taught by Ingrashi will have a larger width than Koga's conductive plug and the silicide contact pad will be in contact with the first contact spacer (207, 102), which will prevent the second contact spacer (209, 109 – Koga's Fig. 10(d) & 6(c)) contacting the silicide contact pad. In other words, since first spacer 207 is positioned under the second spacer 209, only the first spacer will have a contact area with the silicide contact pad.

In view of the above, applicant's arguments are not persuasive.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad Timor Karimy whose telephone number is 571-272-9006. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on 571-272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mtk

/Kimberly D Nguyen/
Supervisory Patent Examiner, Art Unit 2894